electron beam pattern

for smaller, sharper images

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THE COMPLEXITY of silicon integrated circuits has been steadily increasing each year. On a consumer basis, this increase has made economically possible such modern electronic wonders as pocket calculators and electronic wristwatches.

One can assume that the cost of a processed wafer remains relatively unchanged and is independent of the complexity of the devices it carries. Hence, in a mass production environment, the more functions a device manufacturer can design into each device, the lower the cost per function.

As this trend continues, one can expect powerful calculators, for example, that will have capability comparable to that of the large computers of yesterday. These devices then would be available to the general public for the cost of only a few hundred dollars.

It is obvious that the push toward more and more complexity in large scale integrated circuits will never stop. And technological breakthroughs will be sought in the economical production of these increasingly complex devices. One of these technological breakthroughs is happening at this moment—electron beam pattern generation in terms of device lithographic techniques.

One of the major processes in the fabrication of integrated circuits exists in the delineation of circuit elements on the silicon wafer during processing. In the early days of the microfabrication of integrated circuits, pattern data from a device designer was used to generate a large scale plot or layout of each lithographic step during the device fabrication.

This large layout usually is made at 100 to 200 times real size; it subsequently is reduced by high resolution and high accuracy photographic techniques. For modern integrated circuits, the real size of the device often is only a few mm^2.

The reduced pattern then is stepped and repeated on a high precision glass plate to generate arrays of identical patterns, forming a photomask. Subsequently, the photomask is used in the duplication process, transferring the exact pattern to the surface of the wafer coated with photo resist. This procedure is repeated during each of the processing steps in the fabrication of the wafer and eventually results in a silicon wafer full of integrated circuit chips.

Over the years, new and improved procedures and equipment have resulted in fewer steps in the fabrication process for these integrated circuit wafers. And fewer steps usually represent fewer things to go wrong—and hence, less costly end products.

The most recent advance in pattern generation is the optical pattern generator which replaces a large plotter and reduction pho-